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Deterministic Multi-Modal Sensor Ingestion and Actuation via Holoscan-Integrated Switched Fabrics

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ABSTRACT

Modern-day sensors encounter performance bottlenecks due to latency in the data path to processing, analysis, and storage functions. This issue can be mitigated by introducing a direct PCI Express (PCIe) or PCIe-switched fabric connection to the sensor [1]. This white paper presents a hardware-defined architecture that integrates NVIDIA Holoscan [2] with PCIe switch fabrics [6] to provide a unified transport for heterogeneous sensor ingestion, hardware-level multicast routing, and high-performance multiprocessing. By utilizing a Single Root Complex model, a designated Switch Control Processor (SCP) manages global PCIe enumeration and dynamic routing over a native PCIe interface. This enables the fabric to treat diverse sensor interfaces—including VITA 49 RF [3], LIDAR, and EO/IR—and GPUs as peer-to-peer endpoints within a unified, low-latency memory map.

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1. INTRODUCTION

This architecture builds upon work presented at the 2025 Ground Vehicle Systems Engineering and Technology Symposium (GVSETS). In "Sensor Latency Advantage in PCI Express Switched Fabrics" [1], several foundational principles were established:

- **Latency Superiority:** PCIe significantly reduces latency, outperforming other common connection types like Ethernet.
- **High Bandwidth:** A PCIe Gen5 x16-lane interface moves up to 63 GB/s in each direction between devices [6].
- **Switch Versatility:** A PCIe-switched fabric allows selective communication between all devices in the fabric, including hardware-level multicast [1].
- **Hardware-Level Assembly:** With PCIe, payload assembly and

disassembly are handled by the interface itself, making the latency introduced by software negligible compared to the millisecond-level overhead of Ethernet.

As a result of that earlier work, a Rugged PCIe 8-port Fabric Switch with integrated Switch Control Processor has been developed for use in land vehicles, along with companion CPU/GPU components.

Figure 1 - Fabric Switch with SCP

2. SYSTEM ARCHITECTURE

By utilizing a **Single Root Complex** model, a designated Switch Control Processor (SCP) manages global PCIe enumeration and dynamic routing. This enables the fabric to treat diverse sensor interfaces and GPUs as peer-to-peer endpoints within a unified, low-latency memory map. The integration of the NVIDIA Holoscan SDK allows these varied sensor streams to bypass the host CPU entirely, utilizing GPUDirect RDMA to deliver data directly into GPU RAM for real-time fusion and AI-driven analysis. Crucially, this architecture maintains full compatibility with mature, field-proven software libraries, including CUDA and TensorRT, without requiring code modification. By resolving resource contention at the hardware design phase through non-blocking switch topologies, the system ensures deterministic, "line-rate" delivery of mission-critical data across all sensor modalities.

At system startup, the SCP performs a comprehensive discovery of all connected endpoints. By managing this globally, the SCP establishes a flat, unified memory mapped I/O (MMIO) space. All GPUs, CPUs, and sensor interfaces are part of the same hierarchy, enabling the PCIe switch silicon to handle data transfers directly between endpoints. Performance is maximized through non-blocking switch topologies, ensuring the system maintains sub-microsecond latency and predictable throughput.

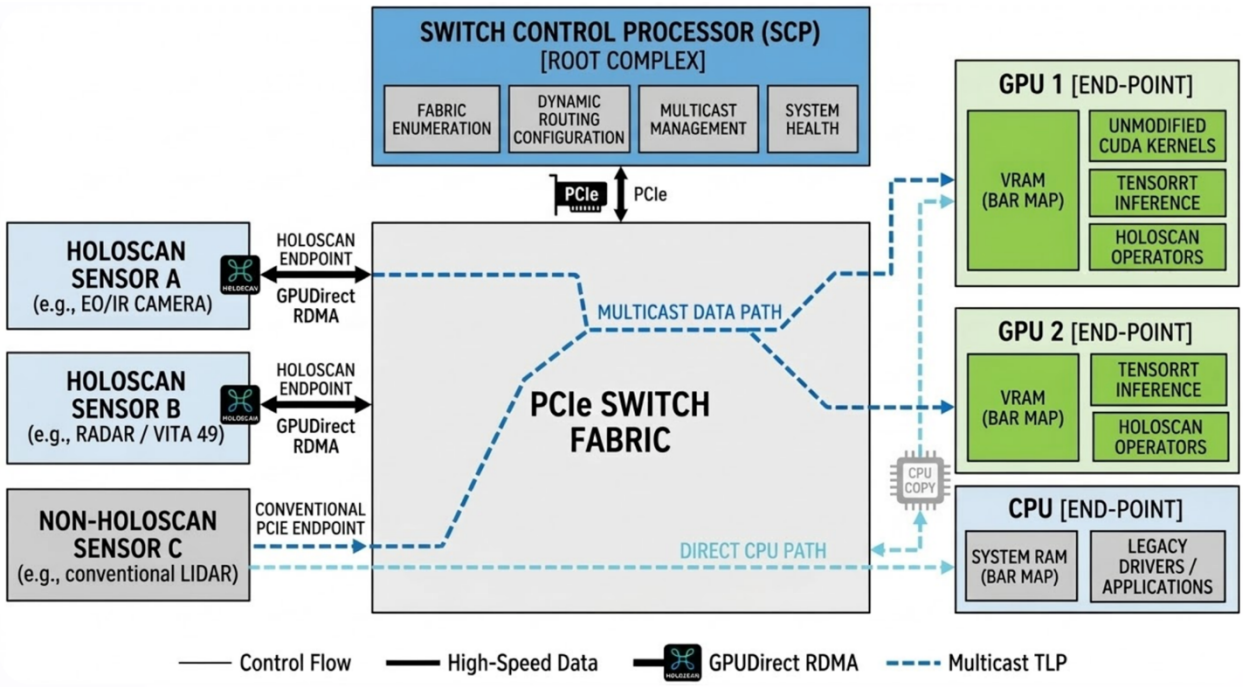

Figure 2 - Fabric Block Diagram

2.1. Ingestion, Multicast, and Symmetry

Once the SCP establishes the initial routing, the Data Plane operates as a purely hardware-driven conduit. For a typical VITA 49 RF sensor, the interface (often a Mellanox NIC) converts incoming streams into PCIe Memory Write Transaction Layer Packets (TLPs).

- **Zero-Buffer Ingress:** Data is streamed directly into the switch fabric without being buffered in the sensor's local memory or a middle-man CPU.
- **Fabric-Level Multicast:** The switch fabric utilizes hardware-level multicast to replicate data packets at the silicon layer. A single feed can be routed to multiple GPUs simultaneously with no cumulative latency.
- **Direct-to-RAM:** The final stage is a direct write into the GPU's high-bandwidth memory.
- **Bidirectional Symmetry:** While Holoscan is primarily regarded as an ingestion framework, the PCIe fabric itself is symmetric and bidirectional. This allows the system to support high-throughput, low-latency **output**—such as pushing processed waveforms from a GPU back across the fabric to a DAC or RF Exciter for electronic attack or counter-measure applications.

2.2. The Switch Control Processor (SCP) and Software Integration

The SCP governs the **Control Plane**, serving as the system's central authority for enumeration, dynamic routing, and health monitoring. By managing these at the hardware level, the SCP presents a stable environment to the **NVIDIA Holoscan.**

The software layer utilizes the **RoCE (RDMA over Converged Ethernet)**

interface to address the data using standard networking semantics, while the physical delivery occurs via PCIe. This ensures compatibility with unmodified software components:

- **CUDA Toolkit:** Executes parallel processing on data already present in local RAM.
- **TensorRT:** Performs real-time AI inference.
- **Holoscan Operators:** Orchestrate the data flow graph without requiring knowledge of the underlying PCIe switch complexity.

3. EW AND C-UAS USE CASES

In the context of **Electronic Warfare (EW)** and **Counter-UAS (C-UAS)**, the transition to a symmetric PCIe fabric combined with NVIDIA Holoscan directly addresses the "Sensor-to-Shooter" (or "Sensor-to-Effector") latency gap. By moving from legacy CPU-centric architectures to a hardware-accelerated data plane, these systems gain the speed and efficiency required to counter modern, fast-moving, or autonomous threats.

3.1. Performance: Closing the Reaction Loop

In EW and C-UAS, performance is measured by the **speed of the decision loop**.

- **Nanosecond-Scale Decision Making:** As noted in the **2025 GVSETS** reference, traditional Ethernet-based ingest adds millisecond-scale jitter and software overhead. In a PCIe fabric, the data arrives at the GPU in microseconds ($<10\mu s$). This allows an EW system to identify a frequency-hopping signal and deploy a countermeasure before the threat changes state.
- **Deterministic Sensor Fusion:** C-UAS requires "layering" (Radar, EO/IR, and SIGINT). Because the fabric is symmetric, all three sensor types can land in a shared GPU memory space simultaneously. The software can fuse this data without the "stutter" caused by CPU interrupts, ensuring the target track is seamless across different sensor modalities.
- **Line-Rate Multicast:** For swarm defense, a single radar detection can be hardware-multicast to multiple effectors (e.g., a high-power microwave, a kinetic interceptor, and a jammer). Each system receives the "Target Detected" TLP at the exact same moment, enabling a coordinated, multi-layered response.

3.2. Reducing SWaP-C (Size, Weight, Power, and Cost)

Traditional military processing racks are heavy and power-hungry because they rely on multiple discrete computers (SBCs) connected by complex backplanes. This architecture consolidates those functions.

- **Consolidation of Hardware:** Because a single PCIe switch handles routing and a single SCP manages the entire fabric, you eliminate the need for redundant Host CPUs and specialized networking switches. This significantly reduces the Size (S) and Weight (W) of the mission computer.
- **Lower Power (P) Density:** Moving data via PCIe TLPs is inherently more power-efficient than "packetizing" data for Ethernet. By using **GPUDirect RDMA** to bypass the CPU, the system reduces the processors' thermal load, allowing for smaller cooling fans or passive heat sinking.

- **Simplified Maintenance (C):** Using **MOSA-compliant** PCIe standards and unmodified software libraries (CUDA, Holoscan) means that components from different vendors can be swapped out. This reduces lifecycle **Cost (C)** by preventing vendor lock-in and allowing for rapid field upgrades without a complete system redesign.

3.3. Symmetrical Actuation for EW

The most profound improvement for EW is the **Symmetric Data Path**.

- **High-Throughput Egress:** Traditional systems struggle to push high-bandwidth waveforms from a GPU back to an antenna. This architecture treats the **Digital-to-Analog Converter (DAC)** as a peer on the PCIe fabric.
- **The Result:** A GPU can generate an complex jamming waveform in local RAM and "push" it directly to the RF Exciter at the speed of the VITA 49 or PCIe bus, enabling true **Digital Radio Frequency Memory (DRFM)** capabilities.

4. A MOSA-COMPLIANT FUTURE

By separating the Control Plane from a symmetric, bidirectional Data Plane, this architecture provides a unified, low-latency ecosystem for sensor fusion and closed-loop "Sensor-to-Effector" operations. The use of unmodified COTS software libraries fulfills the core requirements of the Modular Open Systems Approach (MOSA), enabling rapid technology insertion and providing the warfighter with a deterministic, scalable computational edge.

5. REFERENCES

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